Hardware Description Languages

HDL is a high level language (similar to C, Pascal, Fortran, etc) used to specify the design of electronic circuits.

Modern **hardware compilers** can take a high level description of an electronic circuit (e.g. written in an HDL such as **VHDL**, or **Verilog**,or **ABEL**, etc), and translate it into **configuring bit strings**, which are then used to configure a **programmable chip** (e.g. Xilinx's Virtex chip).Thanks to Moore's Law, the number of programmable logic gates (e.g.AND gates, NAND gates, etc) in today's chips are now in the millions.

With such electronic capacities on a single chip, it is now possible to place whole electronic **systems on a chip**.

VHDL's Capabilities & features

- The language can be *used as an exchange medium between chip vendors and CAD tool users.*
- The language supports *hierarchy.*
- The language *supports flexible design methodologies: top-down, bottom-up, or mixed.*
- The language is *not technology-specific.*
- It supports both *synchronous and asynchronous timing models.*

VHDL's Capabilities & features cont..

- The language is publicly available, human readable, machine readable.
- Various digital modeling techniques such as finite-state machine descriptions, algorithmic descriptions, and boolean equations can be modeled using the language.
- It is an *IEEE and ANSI standard, and therefore, models described using this language are portable.*

VHDL's Capabilities & features cont..

- The language supports *three basic different description styles: structural, dataflow, and behavioral.*
- It supports a wide *range, of abstraction levels ranging from abstract behavioral descriptions to very precise gate-level descriptions.*
- *Arbitrarily large designs can be modeled using the language.*

VHDL's Capabilities & features cont..

- The language has elements that make *large scale design modeling easier, for example, components, functions, procedures, and packages.*
- A model can not only describe the functionality of a design, but can also contain *information about the design itself in terms of user-defined attributes, for example, total area and speed.*

VHDL's Capabilities & features cont..

- Models written in this language can be verified by simulation.
- Provides technology independence:

  VHDL is independent of any technology or process (ASIC,FPGA…)
- Eases communication through standard language: Communication among different designers and different tools
- Easier documentation

Hardware Abstraction

- VHDL is used to describe a model for a digital hardware device.
- This model specifies the external view of the device and one or more internal views.
- The internal view of the device specifies the functionality or structure, while the external view specifies the interface of the device through which it communicates with the other models in its environment.

Hardware Abstraction cont..

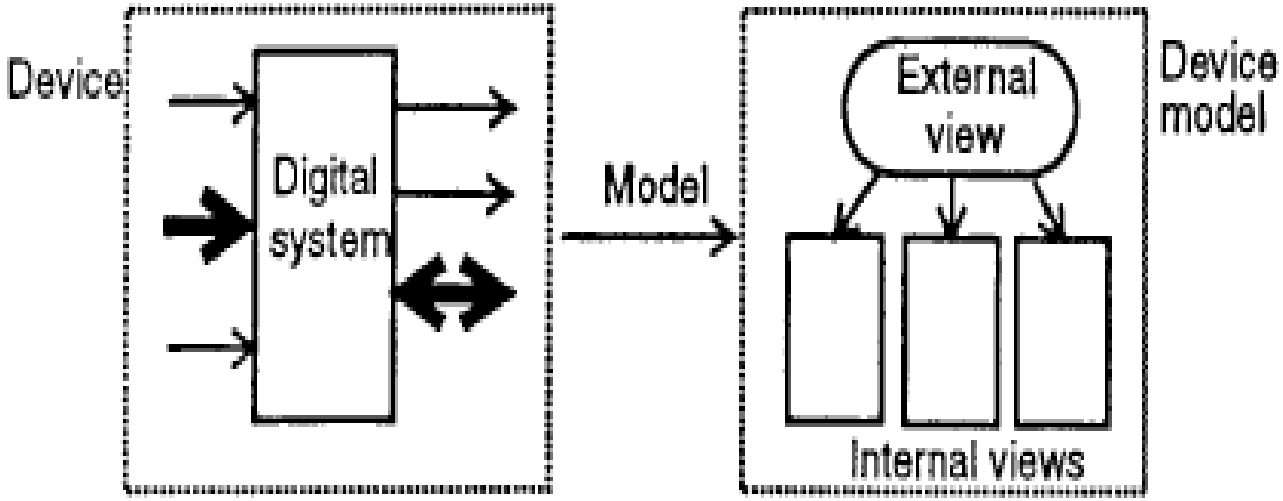

Figure 1.1 Device versus device model.

Hardware Abstraction cont..

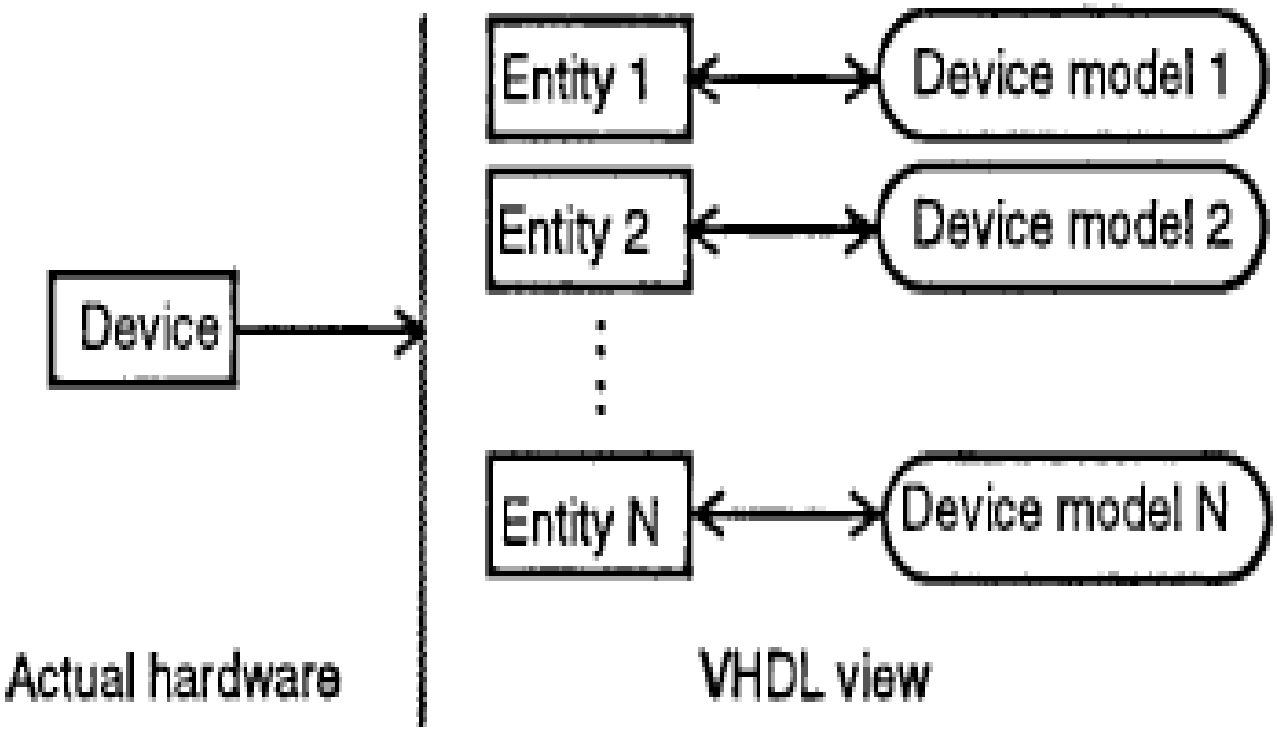

Figure 1.2 A VHDL view of a device.

Hardware Abstraction cont..

- The entity is thus a hardware abstraction of the actual hardware device. Each entity is described using one model that contains one external view and one or more internal views. At the same time, a hardware device may be represented by one or more entities.